Amendments to the Claims:

Please cancel claims 2-43.

Listing of Claims:

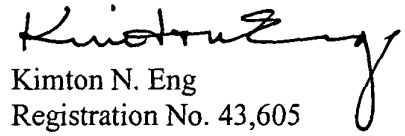
1. (Original) An address predecoder, comprising:

a decoder having input terminals for receiving column memory address signals and further having output terminals for providing initial predecode signals, the decoder selecting one of the output terminals on which to provide an active initial predecode signal based on the column memory address signals; and

a shifting circuit having inputs coupled to the output terminals of the decoder and control terminals for receiving shift control signals, the shifting circuit further having first and second sets of output terminals on which to provide respective column predecode signals, the shifting circuit providing first column predecode signals corresponding to the initial predecode signals on the first set of output terminals and, in response to receiving inactive shift control signals, providing second column predecode signals corresponding to the initial predecode signals and, in response to receiving active shift control signals, reordering the initial predecode signals into a shifted arrangement to be provided on the second set of output terminals as the second column predecode signals.

2-43. (Cancelled)

Respectfully submitted,
DORSEY & WHITNEY LLP



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